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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,003	02/14/2002	Warren Stuart Crippen	2207/12663	6656

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EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

CA

Office Action Summary	Application No.	Applicant(s)	
	10/074,003	CRIPPEN, WARREN STUART	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 10-17 are objected to because of the following: In claims 10, 14 and 17, the limitation "said land grid array side contacts having dimensions and spacing less than said semiconductor side contacts", is misguiding. It seems it is a typographical mistake. Rather, it should be - - the semiconductor side contacts having dimensions and spacing less than said land grid array side contacts - - or "said land grid array side contacts having dimensions and spacing larger than said semiconductor side contacts" Appropriate correction is required.

From the description on page 5 of the specification, paragraph [00017], the land grid array side dimensions are measured in mils and semiconductor side dimensions are measure in microns. As one mil is larger than one micron, it appears that the dimensions, spacing and size, on land grid array side are larger than the dimensions, spacing and size on the semiconductor side.

Also, from figure 7a, it appears that the dimension on side 36, semiconductor side, is smaller than the same on side 34, land grid array side. Further, while comparing the embodiment, figure 7a, with the prior art, figure 7b, paragraph [00030], page 12, it is the thickness which is compared not the spacing on both the sides, and from both the figures 7a and 7b, it appears that, the dimensions, spacing and size, on land grid array side are larger than the dimensions, spacing and size on the semiconductor side.

For the examination purpose, the examiner considered the dimensions, spacing and size, on land grid array side larger than the dimensions, spacing and size, on the semiconductor side.

Claims 11-13, 15 and 17 depend on claims 10, 14 and 16 and inherit the same deficiency.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-12, 14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Pham et al., US Patent No. 6,303,992, hereafter Van, in view of Eldridge et al., US Patent No. 5,974,662.

Regarding claim 10, Van discloses a space transformer comprising:

a silicon medium (interposer body 12 made of ceramic material such a silicon, see figure 4, column 3, line 40-45; and

a predetermined contact pattern comprising electrically conductive material disposed in an inner region of the substrate and defining electrical contact zones located to provide double sided electrical contacts for the space transformer (contact pads 18 and 20 with conductive conduits 22, see figure 4, column 3, line 1-8), but

fails to explicitly disclose land grid array side contacts having dimensions and spacing larger than that on the semiconductor side contacts.

Though, Van discloses a space transformer 12 with semiconductor die 50 connected on one side of the space transformer 12 and a substrate 70 on the other side, with narrower pitch between the contacts on semiconductor side and contacts on the substrate side distributed in larger area, see figure 3A, 3B and 4, column 3, line 40-65.

Eldridge discloses a space transformed 400 with top surface 402a with a relatively fine pitch, about 5-10 mil pitch, center to center spacing comparable to semiconductor die bond pad and bottom surface 402b with terminals at a 50-100 mil pitch, comparable to printed circuit board pitch, land grid array side, see column 23, line 5-25.

A person of ordinary skill in the art at the time the invention was made would readily construe that the dimension, size and spacing, on printed wiring board side, land grid array side would be larger, with wider pitch, than that on the semiconductor side contacts of a space transformer, with narrower pitch, for connecting a semiconductor device on one side of the space transformer and a printed circuit board on the other side of the board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to construe the space transformer of Van, with land grid array side contacts having dimensions and spacing larger than that on the semiconductor side contacts, from the teachings of Eldridge, in order to facilitate connection of the semiconductor device on one side and the printed circuit board on the other side.

Regarding claim 11, the body of Van further discloses a first and second silicon layer with contact pattern being disposed between the first silicon layer and second silicon layer, see figure 4 and 8A-B, column 4, line 60 to column 5, line 5.

Regarding claim 12, the body of Van further discloses the via with electrically conductive material into the via (see figure 4, column 4, line 1-5).

Regarding claim 14, the modified circuit board of Van discloses all the features of the claimed invention, as applied to claim 10-12 above, including the contact pattern comprising copper, column 4,line 1-10.

Regarding claim 16 and 17, the modified circuit board of Van discloses all the features of the claimed invention, as applied to claim 10-12 above, including the means disposed in an inner region located between the first silicon layer and the second silicon

layer, electrically conductive conduits 22, see figure 4, column 3, line 65 to column 4, line 10.

3. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Van and Eldridge, as applied to claims 10-12, 14 and 17 above, and further in view of Petrarca et al., US Patent No. 6,429,522, hereafter, Petrarca and Matsuo et al., US Patent No. 6,614,106, hereafter, Matsuo.

Regarding claim 13, the combination of Van and Eldridge discloses all the features of the claimed invention as applied to claims 10-12, 14 and 17 above, but

fails to disclose an adhesion promoter disposed between the electrically conductive material and the first silicon layer.

Petrarca, in the background discussion, discloses that it is known in the semiconductor industry to apply an adhesion promotion layer such as silicon oxide, silicon nitride, titanium, tungsten or related compounds, before a metal deposition. The adhesion promotion layer is often used as a barrier for metal migration.

Matsuo discloses an interposer 30 made out of silicon substrate, column 2, line 35-50, and adhesion promotion layer for copper plating, column 3, line 23-30.

A person of ordinary skill in the art would readily recognize the advantage of providing adhesion promotion layer, before metal deposition, for better adhesion of the metal.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified structure of Van with adhesion promotion layer, from the teachings of Petrarca and Matsuo, in order to have better adhesion of the metal deposition.

Response to Arguments

4. Applicant's arguments filed on June 23, 2004 have been fully considered but they are not persuasive. The applicant argues that figure 3A and 3B of Van discloses that contacts 20 have dimensions and spacing that are much larger than contacts 18, which is contrary to the new limitations of claim 10, 14 and 16. This is moot as the limitation is not described in the specification and appears a typographical mistake. This has been explained in detail in the objection of the claims.

The applicant further argues that the space transformer of Eldridge is made of ceramic material and is not made of silicon medium as presently claim. However, the secondary art of Eldridge is used for showing the dimensional relation on the both the sides of the transformer only and not for the material of the construction. Also, the applicant argues that Petrarca and Matsuo have been cited for its disclosure of an adhesion promoter. These references, however, fail to make up for the deficiencies of Van and Eldridge references. However, these is the obviousness rejection based on the combination of references. Applicant has performed a piecemeal analysis of the applied prior art. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Keller*, 642 F.2d

413, 208 USPQ 871 (CCPA 1981); *In re Merck* & Co., Inc., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

5. Applicant's amendment necessitated the new ground(s)/ new explanation of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

I B Patel
Examiner
GAU: 2827
July 25, 2004

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800